National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMC6062AM-X REV 0A0

Original Creation Date: 08/16/95
Last Update Date: 10/23/98
Last Major Revision Date: 04/19/96

PRECISION CMOS DUAL MICROPOWER OPERATIONAL AMPLIFIER

General Description

The LMC6062 is a precision dual low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6062 ideally suited for battery powered applications.

Other applications using the LMC6062 include precision fullwave rectifiers, integrators, references, sample-and-hold circuits, and true instrumental amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

Industry Part Number

LMC6062AM

NS Part Numbers

LMC6062AMJ/883

Prime Die

LMC6062

Controlling Document

5962-9209403MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Typical Unless Otherwise Noted)

- Low offset voltage. 100uV
- Ultra low supply current. 16uA/Amplifier
- Operates from 4.5V to 15V single supply.
- Ultra low input bias current. 10fA
- Output swing within 10mV of supply rail, 100k load.
- Input common-mode range includes V-.
- High voltage gain. 140dB
- Improved latchup immunity.

Applications

- Instrumentation amplifier.
- Photodiode and infrared detector preamplifier.
- Transducer amplifiers.
- Hand-held analytic instruments.
- Medical instrumentation.
- D/A converter.
- Charge amplifier for piezoelectric transducers.

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V+ - V-)		16V
Differential Input Voltage		±Supply Voltage
Voltage at Input/Output Pin		(V+)+0.3V,(V-)-0.3V
Current at Input Pin		±10mA
Current at Output Pin		±30mA
Current at Power Supply Pin		40mA
Maximum Junction Temperature		150 C
Power Dissipation (Note 2)		3mW
Output Short Circuit to V+ (Note 4)		
Output Short Circuit to V- (Note 3)		
Storage Temperature Range		-65 C to +150 C
Operating Temperature Range		-55 C ≤ TA ≤ +125 C
Thermal Resistance (Note 6)		
ThetaJA		
8-Pin CERAMIC DIP	(Still Air)	113 C/W
	(500LF/Min Air flow)	51 C/W
ThetaJC		
8-Pin CERAMIC DIP		21 C/W
Lead Temperature (Soldering, 10 seconds)		260 C
ESD Tolerance (Note 5)		2kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: Do not connect output to V+, when V+ is greater than 13V or reliability will be adversely affected.

Note 5: Human body model, 1.5k ohms in series with 100pF.

Note 6: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions
(Note 1)

Supply Voltage

$4.5V \leq V+ \leq 15.5V$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, Vcm = 1.5, V- = 0V, Vo = 2.5V, Rl > 1M

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					350	uV	1
						750	uV	2, 3
Iib	Input Bias Current					25	pA	1
						100	pA	2, 3
Iio	Input Offset Current					25	pA	1
						100	pA	2, 3
CMRR	Common Mode Rejection Ratio	0V <= Vcm <= 12.0V, V+ = 15V			75		dB	1
					70		dB	2, 3
+PSRR	Positive Power Supply Rejection Ratio	5V <= V+ <= 15V, Vo = 2.5V			75		dB	1
					70		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	-10V <= V- <= 0V, Vo = 2.5V			84		dB	1
					70		dB	2, 3
Vcm	Input Common-Mode Voltage Range	V+=5V and 15V for CMRR>=60 dB			V+-2.3	-0.1	V	1
					V+-2.6	0	V	2, 3
Io	Output Current	Sourcing, Vo = 0V			16		mA	1
					8		mA	2, 3
		Sinking, Vo = 5V			16		mA	1
					7		mA	2, 3
		V+ = 15V, Sourcing, Vo = 0V			15		mA	1
					9		mA	2, 3
		V+ = 15V, Sinking, Vo = 13V	1		24		mA	1
			1		7		mA	2, 3
Icc	Supply Current	Both Amplifiers: V+ = +5V, Vo = 1.5V				38	uA	1
						60	uA	2, 3
		Both Amplifiers: V+ = +15V, Vo = 7.5V				47	uA	1
						70	uA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, Vcm = 1.5, V- = 0V, Vo = 2.5V, Rl > 1M

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Avs	Large Signal Voltage Gain	Rl = 100K Ohms, Sourcing	2		400		V/mV	4
			2		200		V/mV	5, 6
		Rl = 100K Ohms, Sinking	2		180		V/mV	4
			2		70		V/mV	5, 6
		Rl = 25K Ohms, Sourcing	2		400		V/mV	4
			2		150		V/mV	5, 6
		Rl = 25K Ohms, Sinking	2		100		V/mV	4
			2		35		V/mV	5, 6
Vop	Output Swing	Rl = 100K Ohms to 2.5V			4.990	.010	V	4
					4.970	.030	V	5, 6
		Rl = 25K Ohms to 2.5V			4.975	.020	V	4
					4.955	.045	V	5, 6
		V+ = 15V Rl=100K Ohms to 7.5V			14.975	.025	V	4
					14.955	.050	V	5, 6
		V+ = 15V Rl=25 K Ohms to 7.5V			14.900	.050	V	4
					14.800	.200	V	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = 5V, Vcm = 1.5, V- = 0V, Vo = 2.5V, Rl > 1M

Sr	Slew Rate	V+ = 15V	3		20		V/mS	4
			3		8		V/mS	5, 6
Gbw	Gain-Bandwidth				80		KHz	4
					75		KHz	5, 6

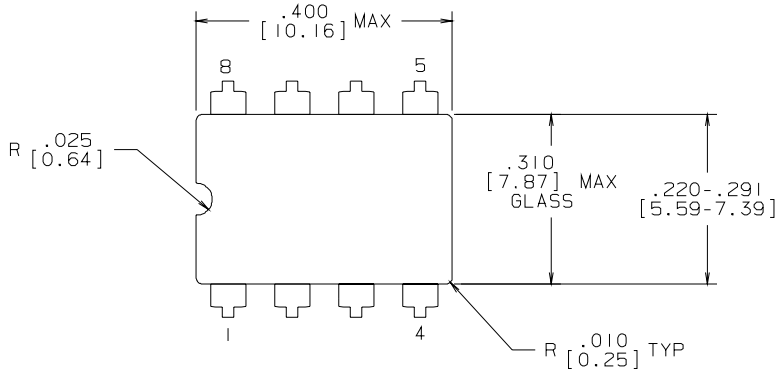
Note 1: Do not short circuit output to V+, when V+ is greater than 13V or reliability will be adversely affected.
Note 2: V+=15V,Vcm=7.5V and Rl connected to 7.5V. For Sourcing tests, 7.5V<=Vo<=11.5V. For Sinking tests, 2.5V<=Vo<=7.5V.
Note 3: Configure for voltage follower, 0 to 10V input step. For +Slew, is measured between 5.5V and 8.0V. For -Slew, is measured between 6.0V and 3.5V.

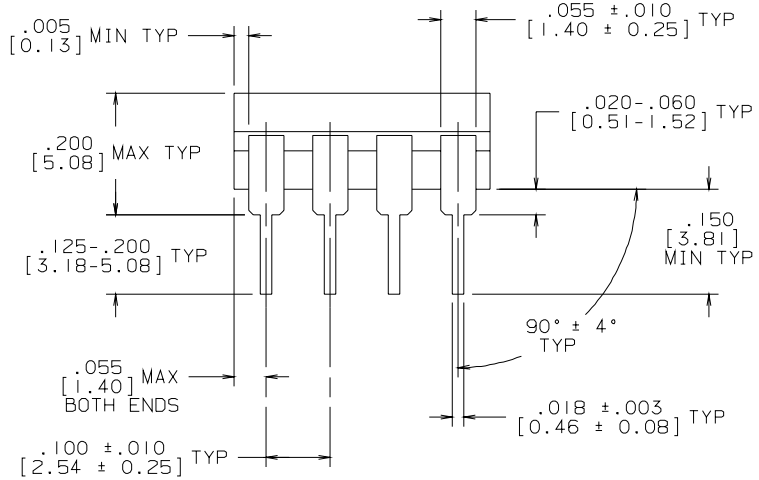
Graphics and Diagrams

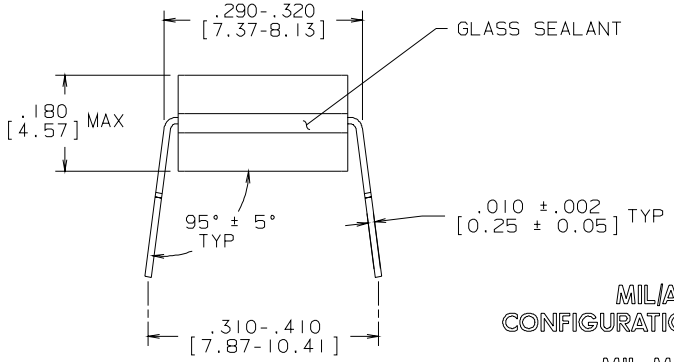
GRAPHICS#	DESCRIPTION
06086HRC4	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000119A	CERDIP (J), 8 LEAD (PIN OUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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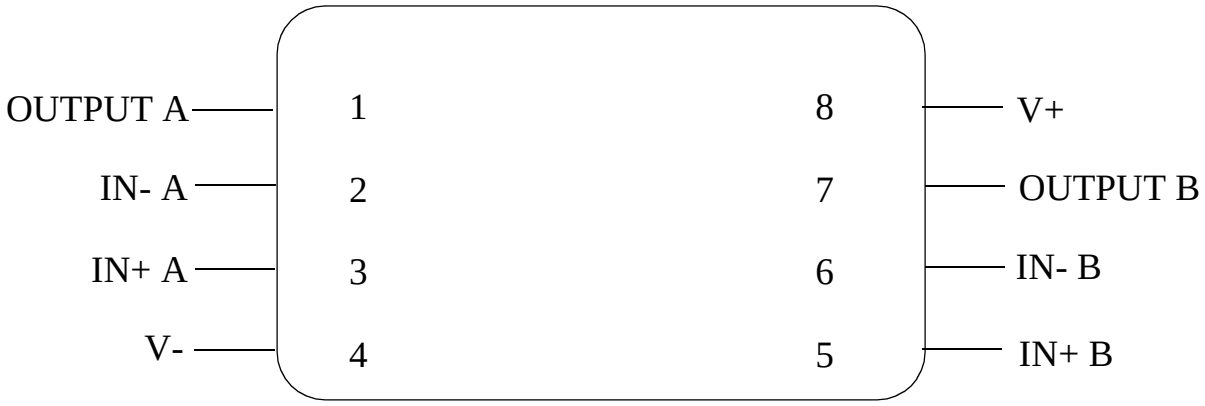
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMC6062J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000119A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002850	10/23/98	Barbara Lopez	Initial Release of MDS: MNLMC6062AM-X Rev. 0A0.